

ABSTRACT OF THE DISCLOSURE

A buffer bypass circuit for reducing latency in information transfers to a bus is described. Access to the bus is governed by a bus arbiter employing a bus parking scheme. The buffer bypass circuit comprises a multiplexer and logic configured such that the information to be transferred is either buffered in a buffer if a grant generated by the bus arbiter indicates that the bus is unavailable, or transferred directly to the bus if the grant indicates that the bus is available and the buffer is empty at the time.